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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,745	03/25/2004	Shoichiro Matsumoto	YKI-0146	9694

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EXAMINER	
SITTA, GRANT	

ART UNIT	PAPER NUMBER
2609	

MAIL DATE	DELIVERY MODE
05/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/810,745	MATSUMOTO, SHOICHIRO	
	Examiner	Art Unit	
	Grant D. Sitta	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/25/2004 and 6/25/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Yumoto et al (6,686,699), hereinafter Yumoto.

3. In regards to claim 1, a current-to-voltage converter circuit (col. 6, lines 30-40, "converting unit") for sequentially converting a current signal (col. 6, lines 30-40, "current") corresponding to a video signal (col. 6, lines 30-40, "data line") for each pixel in a column direction (fig. 10 (121)) into a voltage signal (col. 6, lines 30-40, "for converting the supplied current into a form of voltage");

a data line (fig. 10 (15)) onto which the voltage signal output (fig 10, col. 8, lines 35-65 "Vgs") from the current-to-voltage converter circuit (fig 10 (31)) is sequentially supplied (col. 7-8, lines 50-5, "sequentially driven"); and

a driver element (fig. 10 (32)) provided in each pixel for receiving the voltage signal (col. 9, lines 5-15) from the data line (fig. 10 (15)) on a control terminal (Fig. 10 control line (17)) to control supply of current to the emissive element (col. 9, lines 1-20), wherein the current-to-voltage converter(fig 10, (31)) circuit sets a voltage (col. 8, lines 60-65,

Vgs) on the control terminal of the driver element(fig. 10 (32)) by supplying a current corresponding to a video signal for a selected pixel and supplying a corresponding voltage signal to the data line (col. 9 lines 1-20)

4. In regards to claim 2, each pixel has a storage capacitor (fig. 10 (33)) for accumulating a voltage signal (col. 9, lines 1-20, "33 retains the gate-to-source voltage Vgs of the TFT 31" for the pixel supplied from the data line (fig, 10 (14)), and a current corresponding to the voltage accumulated in the storage capacitor is supplied to the driver element and light is emitted from the emissive element (col. 9, lines 1-5. "TFT 31 converts the voltage retained by the capacitor 33 into a current...")

5. In regards to claim 3, a plurality of data lines (fig. 8, 14-1,14-2, 14-m) are provided and one current-to-voltage converter (fig. 10 (31)) circuit is provided corresponding to each data line. Examiner notes that in fig. 10 TFT 31 and data line 14 share a corresponding node.

6. In regards to claim 4, a plurality of data lines (fig. 8, 14-1,14-2, 14-m) are provided and a plurality of the current-to-voltage converter circuits (fig. 8, 16-1,16-2,16-m) are provided corresponding to each data line (col. 7-8, lines 45-35).

7. In regards to claim 5, one current-to-voltage converter circuit (fig. 8, 16-1) is provided on each of two ends of each data line (fig. 8, circuitry next to 14-1 that is not labeled). Examiner notes that the matrix layout of the el display will have a current-to-voltage converter circuit at the beginning and the end of the data line as long as there is a pixel circuit at the beginning and the end of the data line.

8. In regards to claim 6, the current-to-voltage converter circuit (fig. 10 (31)) comprises a diode-connected transistor (col. 8 lines 50-55, a short circuit caused by TFT 32 between the gate and drain of the TFT (31)) for supplying a current signal corresponding to the video signal, and a voltage on a control terminal of the diode-connected transistor is supplied to the data line (col 8, lines 45-65).

9. In regards to claim 7, the diode-connected transistor has a source connected to a power supply (fig. 10 (31) (ground)) and a gate and a drain connected to the data line (fig. 10 31 connected to 14). Examiner notes that the source is connected to the ground instead of the power supply. However, applicant has not shown any advantage in connecting this way. The energy potential is still across the TFT, therefore, it would have been obvious to one skilled in the art to reverse the polarities.

10. In regards to claim 8, a selection transistor (fig 12 (34)) is placed between the data line (fig. 12 (14)) and the control terminal (Fig. 10 control line (17)) of the driver element in each pixel, and the driver element and the diode-connected transistor (fig. 12 (31)) form a current mirror structure when the selection transistor is switched on (col. 10-11, lines 60-15.)

11. In regards to claim 9, the current-to-voltage converter circuit (fig. 16) comprises a plurality of diode-connected transistors (fig. 16, (31)(37) for supplying a current signal corresponding to the video signal (fig. 14 video signal runs along data lines), and a voltage (Vgs) on a control terminal (Fig. 10 control line (17)) of the plurality of diode-

connected transistors is supplied to the data line (fig. 8 diode-connected transistors at (16-1), (16-2), (16-m)) .

12. In regards to claim 10, the plurality of diode-connected transistors (fig. 8 diode-connected transistors at (16-1), (16-2), (16-m)) have sources connected to a power supply and gates and drains connected to the data line (fig. 10 (31) (ground)). See reasoning in claim 7.

13. In regards to claim 11, see claim 8. Examiner also notes Yumoto teaches using a TFT as a switch in the active matrix method. ("(typically a thin film transistor; TFT)" col. 1, lines 50-55)

14. In regards to claim 12, a converter circuit (col. 6, lines 20-25, "electrooptic device") for receiving a video signal having a voltage indicative of brightness (col. 6, lines 20-30, "changes brightness") and for converting the received signal (col. 6, lines 20-30 "corresponding to brightness...via each data line") into a current signal (col. 6, lines 20-30 "writing current") corresponding to the video signal (col. 6, lines 20-30 via "data line").

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-270-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Grant D. Sitta

April 24, 2007

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER